CLAIMS

1. A method for optimizing cleaning of a probe card including:

using the probe card to test the functionality of dies on a wafer;

when a die fails the probe test, and the probe reports failure to contact the pads of the die, assessing a characteristic of the probe needles; and

if the characteristic of a probe needle is greater than a predetermined value triggering probe needle cleaning.

2. A method for optimizing cleaning of a probe card as claimed in claim 1 wherein the probe needle cleaning is performed by a separate device.

3. A method for optimizing cleaning of a probe card as claimed in claim 1 or claim 2 wherein the tester module controls the probe and probe module.

4. A method for optimizing cleaning of a probe card as claimed in claim 3 wherein the tester is arranged to assess whether the probe test is a pass or a fail.

5. A method for optimizing cleaning of a probe card as claimed in any one of claims 1 to 4 wherein if the test is a fail the tester module is further arranged to determine whether or not to skip the die.

6. A method for optimizing cleaning of a probe card as claimed in claim 5 further including the step of re-probing the die if the die is not skipped.

7. A method for optimizing cleaning of a probe card as claimed in claim 6 wherein if the re-probe produces a fail result, the tester module is further arranged to assess whether the maximum number of dies per clean has been exceeded.

8. A method for optimizing cleaning of a probe card as claimed in claim 7 further including the step of cleaning the probe needles if the maximum number of dies per clean has been exceeded.

9. A method for optimizing cleaning of a probe card as claimed in claim 7 wherein if the maximum number of dies per clean has not been exceeded, the tester module further includes the step of assessing whether the probe is within the minimum number of dies before clean.

10. A method for optimizing cleaning of a probe card as claimed in claim 9 wherein if the probe is within the minimum number of dies before a clean, the tester module further includes the step of instructing the probe to skip to the next die.

11. A method for optimizing cleaning of a probe card as claimed in claim 9 wherein if the probe is above the minimum number of dies before a clean, the tester module further includes the step of assessing whether the maximum number of cleans per wafer has been exceeded.

12. A method for optimizing cleaning of a probe card as claimed in claim 11 wherein if the maximum number of cleans per wafer has been exceeded, the tester module includes the step of instructing the probe to skip to the next die.

13. A method for optimizing cleaning of a probe card as claimed in claim 11 wherein if the maximum number of cleans per wafer has not been exceeded, the tester module further includes the step of checking whether the tester measurement tool is enabled for testing on the probe.

14. A method for optimizing cleaning of a probe card as claimed in claim 13 wherein if the tester measurement tool is enabled for testing on the probe, the tester module includes the step of testing the probe using the tester measurement tool.

15. A method for optimizing cleaning of a probe card as claimed in claim 14 wherein the tester measurement tool tests a characteristic of all pins of the probe.

16. A method for optimizing cleaning of a probe card as claimed in claim 15 wherein if the per pin measurement of a characteristic of the pins passes a predetermined level, the tester module further includes the step of checking the average of the characteristic of the pin measurements.

17. A method for optimizing cleaning of a probe card as claimed in claim 16 wherein if the average pin measurement of the characteristic falls within a predetermined range the tester module is further arranged to instruct the probe to move onto the next die.

18. A method for optimizing cleaning of a probe card as claimed in claim 15 wherein if the per pin measurement of the characteristic falls outside the predetermined range the tester module further includes the step of triggering probe needle cleaning.

19. A method for optimizing cleaning of a probe card as claimed in claim 16 wherein if the average pin measurement of the characteristic falls outside the predetermined range the tester module further includes the step of triggering the probe needle cleaning.

20. A method for optimizing cleaning of a probe card as claimed in claim 14 wherein if the tester measurement tool is not enabled for testing, the tester module further includes the step of using a standard continuity test.

21. A method for optimizing cleaning of a probe card as claimed in any one of claims 1 to 20 wherein the characteristic is resistance.

22. A method for optimizing cleaning of a probe card as claimed in any one of claims 1 to 20 wherein the characteristic is voltage.

23. A system for optimizing cleaning of a probe card including:

a probe card arranged to test the functionality of dies on a wafer;

when a die fails the probe test, the probe card is further arranged to report failures to contact the pads of the die to a tester module, the tester module arranged to assess a characteristic of the probe needles; and

if the characteristic of a probe needle is greater than a predetermined value the tester module is arranged to trigger probe needle cleaning.

24. A system for optimizing cleaning of a probe card as claimed in claim 23 further including a separate device arranged to perform the probe needle cleaning.

25. A system for optimizing cleaning of a probe card as claimed in claim 23 or claim 24 wherein the tester module controls the probe and probe module.

26. A system for optimizing cleaning of a probe card as claimed in claim 25 wherein the tester module is arranged to assess whether the probe test is a pass or a fail.

27. A system for optimizing cleaning of a probe card as claimed in any one of claims 23 to 26 wherein if the test is a fail the tester module is further arranged to determine whether or not to skip the die.

28. A system for optimizing cleaning of a probe card as claimed in claim 27 wherein the tester module is further arranged to instruct the probe to re-probe the die if the die is not skipped.

29. A system for optimizing cleaning of a probe card as claimed in claim 28 wherein if the re-probe produces a fail result, the tester module is further arranged to assess whether the maximum number of dies per clean has been exceeded.

30. A system for optimizing cleaning of a probe card as claimed in claim 29 wherein the tester module is arranged to instruct cleaning the probe needles if the maximum number of dies per clean has been exceeded.

31. A system for optimizing cleaning of a probe card as claimed in claim 29 wherein if the maximum number of dies per clean has not been exceeded, the tester module is further arranged to assess whether the probe is within the minimum number of dies before clean.

32. A system for optimizing cleaning of a probe card as claimed in claim 31 wherein if the probe is within the minimum number of dies before a clean, the tester module is further arranged to instruct the probe to skip to the next die.

33. A system for optimizing cleaning of a probe card as claimed in claim 31 wherein if the probe is above the minimum number of dies before a clean, the tester module is further arranged to assess whether the maximum number of cleans per wafer has been exceeded.

34. A system for optimizing cleaning of a probe card as claimed in claim 33 wherein if the maximum number of cleans per wafer has been exceeded, the tester module is further arranged to instruct the probe to skip to the next die.

35. A system for optimizing cleaning of a probe card as claimed in claim 33 wherein if the maximum number of cleans per wafer has not been exceeded, the tester module is further arranged to check whether the tester measurement tool is enabled for testing on the probe.

36. A system for optimizing cleaning of a probe card as claimed in claim 35 wherein if the tester measurement tool is enabled for testing on the probe, the tester module is further arranged to test the probe using the tester measurement tool.

37. A system for optimizing cleaning of a probe card as claimed in claim 36 wherein the tester measurement tool is arranged to test a characteristic of all pins of the probe.

38. A system for optimizing cleaning of a probe card as claimed in claim 37 wherein if the per pin measurement of a characteristic of the pins passes a predetermined level, the tester module is further arranged to assess the average of the characteristic of the pin measurements.

39. A system for optimizing cleaning of a probe card as claimed in claim 38 wherein if the average pin measurement of the characteristic falls within a predetermined range the tester module is further arranged to instruct the probe to move onto the next die.

40. A system for optimizing cleaning of a probe card as claimed in claim 37 wherein if the per pin measurement of the characteristic falls outside the predetermined range the tester module is further arranged to trigger probe needle cleaning.

41. A system for optimizing cleaning of a probe card as claimed in claim 38 wherein if the average pin measurement of the characteristic falls outside the predetermined range the tester module is further arranged to trigger the probe needle cleaning.

42. A system for optimizing cleaning of a probe card as claimed in claim 36 wherein if the tester measurement tool is not enabled for testing, the tester module is further arranged to use a standard continuity test.

43. A system for optimizing cleaning of a probe card as claimed in any one of claims 23 to 42 wherein the characteristic is resistance.

44. A system for optimizing cleaning of a probe card as claimed in any one of claims 23 to 42 wherein the characteristic is voltage.